AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listing, of claims in the application:

Listing of Claims

1-17. (Canceled without Prejudice)

18. (Currently Amended) A method of reducing stress across an output circuit, comprising:

determining if the output circuit is tri-stated;

determining if a PAD voltage is greater than a predetermined voltage level;

enabling the output circuit;

turning on a stress circuit comprising at least one p-channel transistor, dissipating a voltage across the output circuit, wherein the at least one p-channel transistor comprises a first p-channel transistor and a second p-channel transistor, wherein a drain of the first p-channel transistor is coupled to a source of the second p-channel transistor; and

preventing the output circuit from experiencing HCI stress.

19-21. (Cancelled)

22. (Previously Presented) The method of Claim 18, wherein said at least one p-channel transistor is coupled to the output circuit.

Claim 23 is cancelled without prejudice.

24. (Previously Presented) The method of Claim 18, wherein the output circuit comprises at least one n-channel output transistor.

25. (Previously Presented) The method of Claim 18, wherein the output circuit comprises two stacked n-channel output transistors.

26. (Previously Presented) An HCI stress circuit coupled to both an output circuit and an IO pad, the HCI stress circuit consisting of two stacked p-channel transistor devices, said two stacked p-channel transistor devices adapted to limit a duration of a high voltage across the output circuit thereby reducing hot carrier injection stress across the output circuit.

27. (Previously Presented) The HCI stress circuit of Claim 26, wherein at least one of said two stacked p-channel transistor devices is coupled to the output circuit.

28. (Previously Presented) The HCI stress circuit of Claim 26, wherein the output device comprises at least one n-channel output transistor circuit.

29. (Previously Presented) The HCI stress circuit of Claim 26, wherein the output device comprises two stacked n-channel output transistor circuit.